Patent Claims

1. Conversion arrangement (1) for converting a binary input signal corresponding to an n-bit thermometer code (in(0) - in(15)) into a binary output code (out(0) - out(3)) different therefrom,
having a first number of OR gate circuits (2, 3, 4), into the inputs of which bits of the thermometer code (in(0) - in(15)) can be coupled,
having a first adder (5), which is connected downstream of the OR gate circuits (2, 3, 4) and into the inputs (A, B, C) of which the output signals of the OR gate circuits (2, 3, 4) can be coupled and which provides at least one binary output signal (out(2), out(3)) for the output code (out(0) - out(3)) at its outputs (CO, S),
having a second number of multiplexer circuits (6, 7, 8), into the inputs (I0 - I3) of which bits of the thermometer code (in(0) - in(15)) can be coupled and into the multiplexer selection terminals (S0, S1) of which the output signals (out(2), out(3)) of the first adder (5) can be coupled,
having a second adder (9), which is connected downstream of the multiplexer circuits (6, 7, 8) and into the inputs (A, B, C) of which the output signals of the multiplexer circuits (6, 7, 8) can be coupled and which provides at least one further binary output signal (out(0), out(1)) for the output code (out(0) - out(3)) at its outputs (CO, S).

2. Conversion arrangement according to Claim 1, characterized
in that the number of OR gate circuits (2, 3, 4) and/or the number of multiplexer circuits (6, 7, 8) or the number of the input terminals thereof is defined by the thermometer code (in(0) - in(15)) subdivided into m segments.

3. Conversion arrangement according to one of the preceding claims,
characterized
in that the segments of the thermometer code (in(0) - in(15)) have an identical bit width k, in particular a bit width of k=4 bits.

4. Conversion arrangement according to one of the preceding claims,
characterized
in that the OR gate circuits (2, 3, 4) are designed in such a way that in each case only bits of a single segment can be coupled into the input terminals of a respective OR gate circuit (2, 3, 4).

5. Conversion arrangement according to one of the preceding claims,
characterized
in that the multiplexer circuits (6, 7, 8) are designed in such a way that in each case only bits of different segments, which, however, have the same MSB or LSB significance within the respective segment, can be coupled into the input terminals (IO - I3) of a respective multiplexer circuit (6, 7, 8).

6. Conversion arrangement according to one of the preceding claims,
characterized
in that, in the case of m segments, the first number amounts to m, in particular m-1.

7. Conversion arrangement according to one of the preceding claims,
characterized
in that, in the case of a bit width k of a segment, the second number amounts to k, in particular k-1.

8. Conversion arrangement according to one of the preceding claims,
characterized
in that, in the case of m segments having the bit width 4, the number of input terminals (A, B, C) of the adders (5, 9) amounts at most to m, in particular m-1.

9. Conversion arrangement according to one of the preceding claims,
characterized
in that at least one adder (5, 9) is designed as a full adder.

10. Conversion arrangement according to one of the preceding claims,
characterized
in that the adders (5, 9) and/or the OR gate circuits (2, 3, 4) and/or the multiplexer circuits (6, 7, 8) have a circuit construction of a standard cell from a digital circuit library.

11. Conversion arrangement according to one of the preceding claims,
characterized
in that the converter (1) has n input terminals and m output terminals (10 - 13).

12. Conversion arrangement according to one of the preceding claims,
characterized
in that the binary output code (out(0) - out(3)) is a binary code or a hexadecimal code.

13. Method for converting a binary input signal corresponding to a thermometer code (in(0) - in(15)) into a binary output code (out(0) - out(3)) different therefrom,
having the following method steps:

(a) an n-bit thermometer code (in(0) - in(15)) is provided;

(b) the n-bit thermometer code (in(0) - in(15)) is subdivided into m segments;

(c) the bits of at least the m-1 more significant segments (MSB) are in each case ORed;

(d) the at least m-1 output signals from the ORing are added up, the binary result from this addition forming a first, more significant part of the output code (out(2), out(3));

(e) bits of different segments, which, however, have the same MSB or LSB significance within the respective segment, are multiplexed with one another, the first part of the output code (out(2), out(3)) being used as multiplex selection signal;

(f) the multiplexed output signals are added up, the binary result from this addition forming a second, less significant part of the output code (out(0), out(1)).

14. Method according to Claim 13,
characterized
in that only the bits of the more significant segments (MSS), but not the bits of the least significant segment (LSS) are used for the ORing.

15. Method according to one of Claims 13 to 14,
characterized
in that only the MSB bits of a segment, but not the LSB bit, are used for the multiplexing.

16. Method according to one of Claims 13 to 15,
characterized
in that
OR gate circuits (2, 3, 4) are used for the ORing and/or multiplexer circuits (6, 7, 8) are used for the multiplexing, the number of OR gate circuits (2, 3, 4) and/or the number of multiplexer circuits (6, 7, 8) or the number of the input terminals thereof being defined

by subdivision of the thermometer code (in(0) - in(15)) into m segments.

17. Method according to one of Claims 13 to 16, characterized
in that the thermometer code (in(0) - in(15)) is subdivided into m segments each having the same bit width k, in particular the bit width k=4.

18. Method according to one of Claims 13 to 17, characterized
in that
the binary output code (out(0) - out(3)) is a binary code or hexadecimal code.

19. Analog-to-digital converter (20),
- having at least one analog input (21) for coupling at least one analog input signal (VI) into an input stage (22),
- having a reference stage (23, 24), which is connected downstream of the input stage (22) and provides an n-bit thermometer code (in(0) - in(15)) on the output side from the output signals of the input stage (22),
- having at least one converter arrangement according to one of Claims 1 to 12 or having at least one coder (1) for carrying out a method according to one of Claims 13 to 18, and
- having at least one digital output (10-13) for providing digital output signals (out(0) - out(3)) for the binary output code.

20. Analog-to-digital converter according to one of Claims 19 to [sic],
characterized
in that the analog-to-digital converter (20) is designed as a parallel analog-to-digital converter or as a flash analog-to-digital converter.